

ASM2362 Data Sheet

USB3.1 Gen2 to PCI Express Gen3 x2 NVMe
device bridge

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Environmentally hazardous materials are not used in this product.

Revision History

Rev.	Date	Description
0.1	December 20, 2017	Initial Release
0.2	March 14, 2018	Update the pinout and correct the typo for pin description
0.3	June 25, 2018	Update the electrical specification and power on sequence and package information

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1. General Description

ASM2362 is ASMedia first generation PCI Express(downstream port) to USB3.1(UFP) controller, featuring PCI Express Gen3 x2 and one USB3.1 Gen2 device port, providing high bandwidth up to 10Gbps between PCI Express Gen3 x2 bus and USB 3.1 SuperSpeedPlus bus. It uses for external USB3.1 Gen2 NVM Express SSD application without proprietary additional driver, reaching over 1000MB/s excellent benchmark performance, integrating USB 10Gbps mux and Configuration Channel bus for type-C connector, supporting PCI Express M.2 socket and SSD U.2 form factor, saving power consumption through USB and PCI Express Link power management and Chip power management, compliant with NVM Express revision 1.2.1, PCI Express Base Spec Revision 3.1a, USB3.1 Revision 1.0 and USB type-C Revision 1.3.

ASM2362 is highly integrated with ASMedia USB3.1 Gen2 and PCI Express Gen3 self-designed PHYs, supplying 3.3V and 1.05V voltage, applying local 25MHz crystal, using 9x9 QFN64 RoHS Green package, supporting variable GPIOs for customized function. Target applications is for USB3.1 Gen2 NVM Express SSDs for high performance external SSD or on board SSD on PC, laptop, servers, docking stations and embedded system.

2. Features

General Feature

- ◇ USB to PCI Express NVMe SSD bridge
- ◇ Integrated 10Gbps mux for type-C application
- ◇ Integrated CC Logic for type-C application
- ◇ Support SPI interface with external ROM for customized RAM code
- ◇ Support I2C and GPIOs and UART interface
- ◇ Internal 3.3V to 2.5V LDO
- ◇ Local 25MHz crystal

Universal Serial Bus Feature

- ◇ Support up to USB3.1 Gen2
- ◇ Support BOT and UAS Protocol
- ◇ Support USB Link power management
- ◇ Support USB Hot Plug
- ◇ Support Spread Spectrum Clock Control
- ◇ Support unmap command set
- ◇ Support ATA passthrough command set
- ◇ Compliant with Universal Serial Bus 3.1 Revision 1.0
- ◇ Compliant with USB Type-C spec Release 1.3

PCI Express Feature

- ◇ Support up to PCI Express Gen3 x2
- ◇ Support PCI Express NVMe SSD without driver
- ◇ Support Spread Spectrum Clock Control
- ◇ 100MHz differential reference clock output
- ◇ Support variable types of PCI Express socket including M.2 and U.2 and so on.
- ◇ Support PCI Express Link power management
- ◇ Compliant with PCI Express base spec Revision 3.1a
- ◇ Compliant with PCIe M.2 Revision 1.0

NVM Express Feature

- ◇ Support NVMe power management
- ◇ Support Standard Vendor Specific Command Format
- ◇ Support NVMe Error Reporting & Recovery
- ◇ S.M.A.R.T drive monitoring
- ◇ Compliant with NVMe Revision 1.2.1

Package Type

- ◇ Green Package 9x9 mm2 QFN 64 (Pb-free)
- ◇ RoHS Compliance

3. Functional Diagram

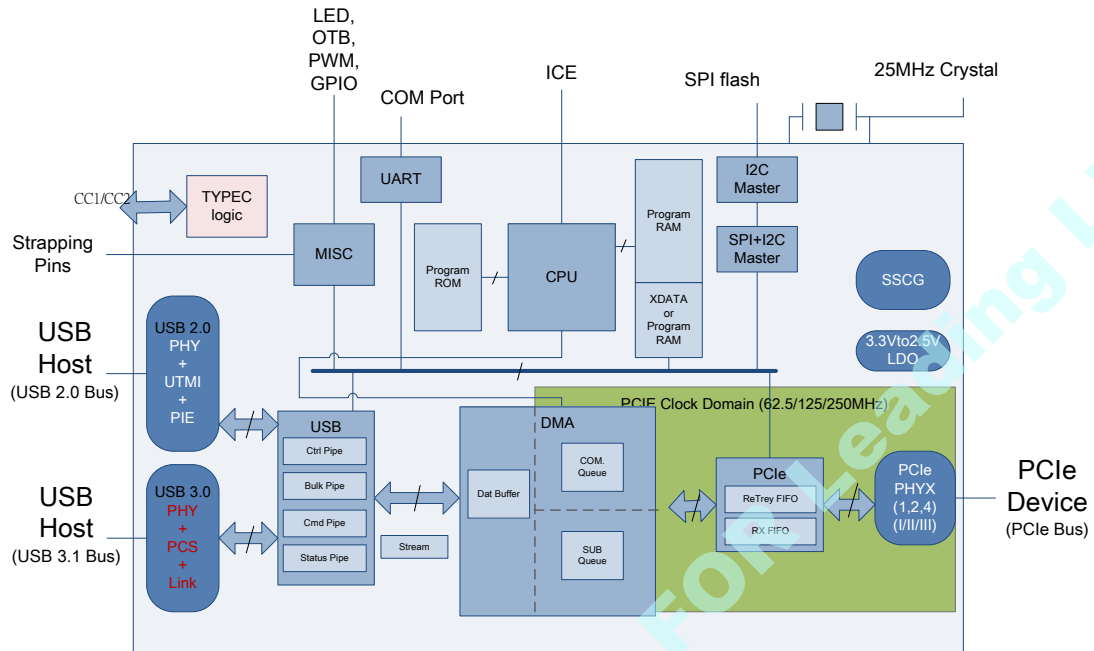


Figure 1: Functional Diagram of ASM2362

4. Pinout Diagrams

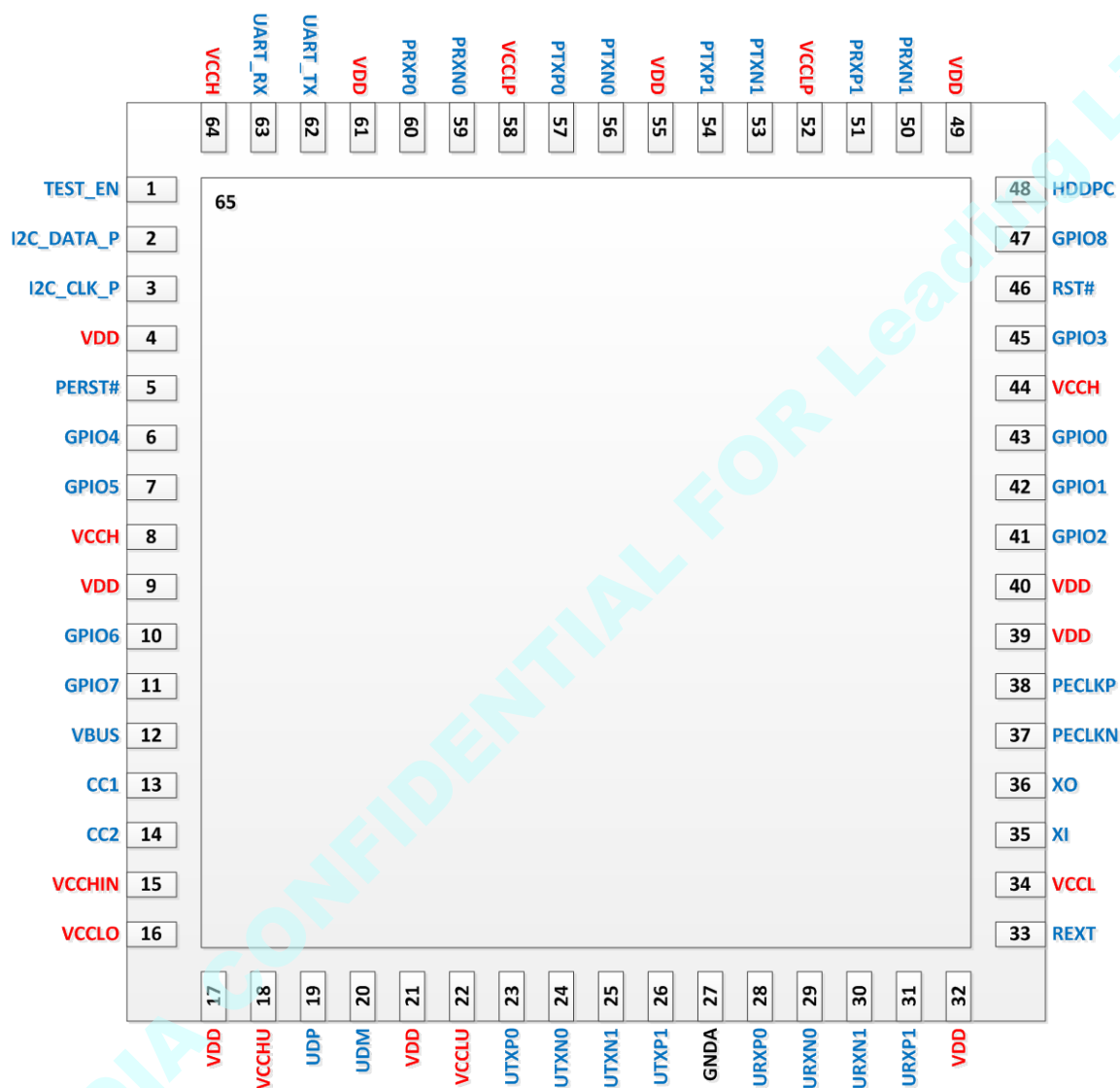


Figure 2: ASM2362 pinout

5. Pin Descriptions

This section provides a detailed description of each signal. The following notations are used to describe the signal type.

I/O Type	Definition
I	Input pin
O	Output pin
B	Bi-directional pin
Di	Differential pin
P	Power pin
G	Ground pin
OD	Open Drain

Pin name	Pin NO.	TYPE	Power	Descriptions
UDP	19	IO	VCCHU	Positive Signal of USB2.0 on Type-C
UDM	20	IO	VCCHU	Negative Signal of USB2.0 on Type-C
UTXP0	23	Di O	VCCLU	Positive Signal of SuperSpeed USB Lane 0 Transmitter for Type-C Configuration Channel 1
UTXN0	24	Di O	VCCLU	Negative Signal of SuperSpeed USB Lane 0 Transmitter for Type-C Configuration Channel 1
UTXP1	26	Di O	VCCLU	Positive Signal of SuperSpeed USB Lane 1 Transmitter for Type-C Configuration Channel 2
UTXN1	25	Di O	VCCLU	Negative Signal of SuperSpeed USB Lane 1 Transmitter for Type-C Configuration Channel 2
URXP0	28	Di I	VCCLU	Positive Signal of SuperSpeed USB Lane 0 Receiver for Type-C Configuration Channel 1
URXN0	29	Di I	VCCLU	Negative Signal of SuperSpeed USB Lane 0 Receiver for Type-C Configuration Channel 1
URXP1	31	Di I	VCCLU	Positive Signal of SuperSpeed USB Lane 1 Receiver for Type-C Configuration Channel 2
URXN1	30	Di I	VCCLU	Negative Signal of SuperSpeed USB Lane 1 Receiver for Type-C Configuration Channel 2
VBUS	12	I	VCCH	USB VBUS input
CC1	13	I	VCCH	Configuration Channel 1 for USB Lane 0 on Type-C
CC2	14	I	VCCH	Configuration Channel 2 for USB Lane 1 on Type-C
PECLKN	37	Di O	VCCLP	Negative Signal of PCI Express Differential Clock
PECLKP	38	Di O	VCCLP	Positive Signal of PCI Express Differential Clock
PRXN1	50	Di I	VCCLP	Negative Signal of PCI Express Lane 1 Receiver
PRXP1	51	Di I	VCCLP	Positive Signal of PCI Express Lane 1 Receiver
PRXN0	59	Di I	VCCLP	Negative Signal of PCI Express Lane 0 Receiver
PRXP0	60	Di I	VCCLP	Positive Signal of PCI Express Lane 0 Receiver
PTXN1	53	Di O	VCCLP	Negative Signal of PCI Express Lane 1 Transmitter
PTXP1	54	Di O	VCCLP	Positive Signal of PCI Express Lane 1 Transmitter
PTXN0	56	Di O	VCCLP	Negative Signal of PCI Express Lane 0 Transmitter
PTXP0	57	Di O	VCCLP	Positive Signal of PCI Express Lane 0 Transmitter
PERST#	5	I	VCCH	Reset Signal for PCI Express interface
RST#	46	I	VCCH	Power on Reset
TEST_EN	1	I	VCCH	Test enable pin, internal weak pull down
I2C_DATA_P	2	IO	VCCH	I2C data, internal weak pull high
I2C_CLK_P	3	IO	VCCH	I2C clock, internal weak pull high
GPIO0	43	IO	VCCH	GPIO0, internal weak pull high
GPIO1	42	IO	VCCH	GPIO1, internal weak pull high
GPIO2	41	IO	VCCH	GPIO2, internal weak pull high
GPIO3	45	IO	VCCH	GPIO3, internal weak pull high
GPIO4	6	IO	VCCH	GPIO4, SPI Chip Select when external SPI flash attach,

				internal weak pull high
GPIO5	7	IO	VCCH	GPIO5, SPI data output when external SPI flash attach, as strapping pin for "SKT_DET" when power on. Please refer to strapping table. Internal weak pull high
GPIO6	10	IO	VCCH	GPIO6, SPI clock output when external SPI flash attach, internal weak pull high
GPIO7	11	IO	VCCH	GPIO7, SPI data input when external SPI flash attach, internal weak pull high
GPIO8	47	IO	VCCH	GPIO8, internal weak pull high
UART_TX	62	I	VCCH	UART transmitter, as strapping pin for "MEMREPAIR" when power on. Internal weak pull high
UART_RX	63	O	VCCH	UART receiver, Internal weak pull high
HDDPC	48	O	VCCH	Power control for NVMe SSD, internal weak pull high
REXT	33	I	VCCH	External resistor 12.1 kohm+/-1%
XI	35	I	VCCH	Crystal Input
XO	36	O	VCCH	Crystal Output
VCCHIN	15	P	VCCH	Regulator Input with VCCH
VCCLO	16	P	VCCL	Regulator output to supply VCCL
VDD	4, 9, 17, 21, 32, 39, 40, 49, 55, 61	P	VDD	Core power supply input
VCCL	34	P	VCCL	Low voltage VCC power input
VCCLU	22	P	VCCL	Low voltage VCC power input for USB
VCCLP	52, 58	P	VCCL	Low voltage VCC power input for PCI Express
VCCH	8, 44, 64	P	VCCH	High voltage VCC power input
VCCHU	18	P	VCCH	High voltage VCC power input for USB PHY
GNDA	27	G		Analog Ground

Strapping Table

Function control for PCIe Hot plug support

GPIO5	SKT_DET
H	Support
L	Not support

Function control for internal memory repair

UART_TX	MEMREPAIR
H	Enable
L	Disable

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Stresses the below parameter listed under absolute maximum rating may cause the device permanent damage. This is a stress rating only, and the function operating of the device at these or any other conditions over those parameter in the recommended operating condition is not implied. It is recommended to have a clamp circuit to protect the device with abnormal exhibit voltage spikes while power is switched on or off.

Parameter	Range	Unit
Power Supply	-0.5 ~ VCC+0.5	V
DC Input Voltage	-0.5 ~ VCC+0.5	V
Output Voltage	-0.5 ~ VCC+0.5	V
Storage Temperature	JEDEC J-STD-033B MSL 3	

6.2 Recommended Operating Conditions

Symbols	Parameter	Min.	Typ.	Max.	Units	Remark
V _{CCH}	High voltage VCC power supply	3.0	3.3	3.6	V	
V _{CCHU}	High voltage VCC power supply for USB	3.0	3.3	3.6	V	
V _{CCL}	Low voltage VCC power supply	2.3	2.5	2.7	V	
V _{CCLU}	Low voltage VCC power supply for USB	2.3	2.5	2.7	V	
V _{CCLP}	Low voltage VCC power supply for PCIe	2.3	2.5	2.7	V	
V _{DD}	Core power supply	1.00	1.05	1.1	V	
T _C	Operating Case Temperature	0		85	°C	
T _J	Silicon Junction Temperature	0	25	120	°C	
HBM	Human Body mode		2		KV	

6.2.1 Chip Temperature (T_J, T_C) Calculation

Symbols	Parameter	How to get?
T _A	Ambient temperature	Measure temperature around chip
T _J	Operating junction temperature	$T_J = \Theta_{JA} * \text{Power} + T_A$
T _C	Operating case temperature	$T_C = T_J - \Psi_{JT} * \text{Power}$
R _{JA}	Junction to Ambient thermal resistance	20.3 (data from package vender)
R _{JC}	Junction to case thermal resistance	4.2 (data from package vender)
Ψ _{JT}	Junction to top thermal characterization	0.07 (data from package vender)
Power	Chip power consumption	Measure chip power consumption

- Thermal test board condition, please refer to JEDEC JESD51-5
- Thermal test method environmental conditions refer to JESD51-2
- Example: If chip power consumption is 1.365W; T_A=57°C
 $T_J = 20.3 * 1.365 + 57 = 84.71^{\circ}\text{C} < 120^{\circ}\text{C}$
 $T_C = 84.71 - 0.07 * 1.365 = 84.61^{\circ}\text{C} < 85^{\circ}\text{C}$

6.3 AC/DC Characteristics

6.3.1 PCI Express Electrical Specification

(Refer to PCI Express Base Specification Rev. 3.0)

6.3.2 USB3.1 Electrical Specification

(Refer to Universal Serial Bus 3.1 Specification Rev. 1.0)

6.3.3 USB2.0 Electrical Specification

(Refer to Universal Serial Bus Specification Rev. 2.0)

6.3.4 DC Electrical Characteristics for digital pins

(Including VBUS, PERST, I2C, UART, HDDPC and GPIOs)

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage Level	2.0			V
V_{IL}	Input Low Voltage Level			0.8	V
V_{HYS}	Input Hysteresis	0.32	0.37	0.4	mV
V_{TH-L2H}	Threshold of Schmitt Trigger low to high	1.4	1.6	1.8	V
V_{TH-H2L}	Threshold of Schmitt Trigger high to low	1	1.23	1.4	V
V_{OH}	Output High Voltage Level	2.4			V
V_{OL}	Output Low Voltage Level			0.4	V
I_{OH}	Output Driving Current while V_{OH}	12			mA
I_{OL}	Output Driving Current while V_{OL}	12			mA
R_{UP}	Internal Pull-up resistance while $V_{in}=0V$	65	96	140	K Ω
	Internal Pull-up resistance while $V_{in}=VCC/2$ V	38	56	81	K Ω
R_{DN}	Internal Pull-down resistance while $V_{in}=VCC$	59	96	142	K Ω
	Internal Pull-down resistance while $V_{in}=VCC/2$ V	35	55	79	K Ω
I_{IL-UP}	Input pull-up leakage current after V_{in} is read, R_{up} is off & $I_{il} < 1\mu A$ when $V_{IN}=0$	21	34.4	56	μA
	Input pull-up leakage current after V_{in} is read, R_{up} is off & $I_{il} < 1\mu A$ when $V_{IN}=VCC/2$	18	29.4	47	μA
I_{IL-DN}	Input pull-down leakage current after V_{in} is read, R_{dn} is off & $I_{il} < 1\mu A$ when $V_{IN}=VCC$	21	34.5	60	μA
	Input pull-down leakage current after V_{in} is read, R_{dn} is off & $I_{il} < 1\mu A$ when $V_{IN}=VCC/2$	18	30	50	μA

6.3.4 DC Electrical Characteristics for RST# pin

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage Level	2.6			V
V_{IL}	Input Low Voltage Level			1.4	V
V_{HYS}	Input Hysteresis	0.21	0.23	0.25	mV
V_{TH-L2H}	Threshold of Schmitt Trigger low to high	1.9	2.2	2.55	V
V_{TH-H2L}	Threshold of Schmitt Trigger high to low	1.65	1.97	2.35	V
Input	Input pull-up leakage current while $V_{in}=0V$			1	mA

6.3.5 External Crystal Electrical Specification

Symbols	Parameter	Min.	Typ.	Max.	Units
f_{XTAL}	Frequency		25		MHz
Δf_{XTAL}	Long Term Stability (at 250C)	-30		30	ppm
t_c	Temperature Stability	-30		30	ppm
F_A	Aging	-5		5	ppm
C_L	Load Capacitance (Single-end mode)		16		pF
C_0	Shunt Capacitance	1	3	7	pF

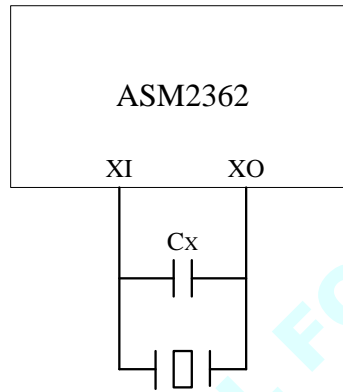


Figure 3: Differential Crystal Design

6.3.6 Differential Clock Oscillator Electrical Specification

Note: The table describes the specification of clock with external 25MHz crystal. Please refer to figure 3.

Symbols	Parameter	Min.	Typ.	Max.	Units
f_{XTAL}	Frequency		25		MHz
Δf_{XTAL}	Long Term Stability (at 250C)	-150		150	ppm
C_x	External Load Capacitance (Differential mode)		10		pF
C_{TATAL}	Total external equivalent Capacitance from XI pin to XO pin (Differential mode)	9	11	15	pF
R_{TOTAL}	Total external equivalent Series Resistance from XI pin to XO pin (Differential mode)			60	Ω

6.3.7 PCI Express 100MHz Output Clock Electrical Specification

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{OH}	Differential Output High Voltage	150			mV
V_{OH}	Differential Output Low Voltage			-150	mV
V_{CROSS}	Absolute crossing point voltage	250		550	mV
t_{CROSS_DELTA}	Variation of V_{CROSS} over all rising clock edges			140	mV
t_{PERIOD_AVG}	Average clock period accuracy	-300		300	ppm
t_{CCJ}	Cycle to Cycle Jitter			150	Ps
t_{DC}	Reference Duty Cycle	40		60	%
$R_{TRISING}$	Rising Edge Rate	0.6		4.0	V/ns
$R_{TFALLING}$	Falling Edge Rate	-4.0		-0.6	V/ns

6.3.8 Internal Linear Regulator Electrical Specification

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{IN}	Input Voltage Range	3.0	3.3	3.6	V
V_{OUT}	Output Voltage Range	2.3	2.5	2.7	V
I_{MAX}	Maximum capacity of current			300	mA

6.3.9 Power Consumption Specification

Symbols	Parameter	Max.	Units
I_{CCHMAX}	Maximum Current consumption of V_{CCH}	8	mA
I_{CCLMAX}	Maximum Current consumption of V_{CCL}	165	mA
I_{DDMAX}	Maximum Current consumption of V_{DD}	530	mA

7. Power on Sequence

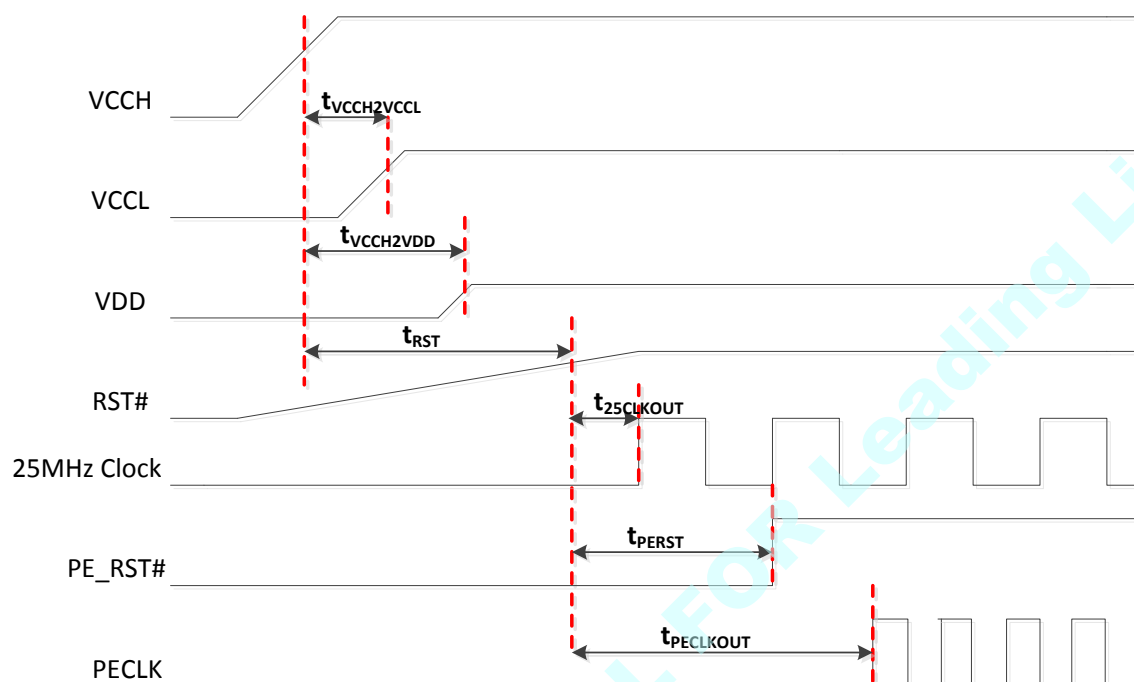
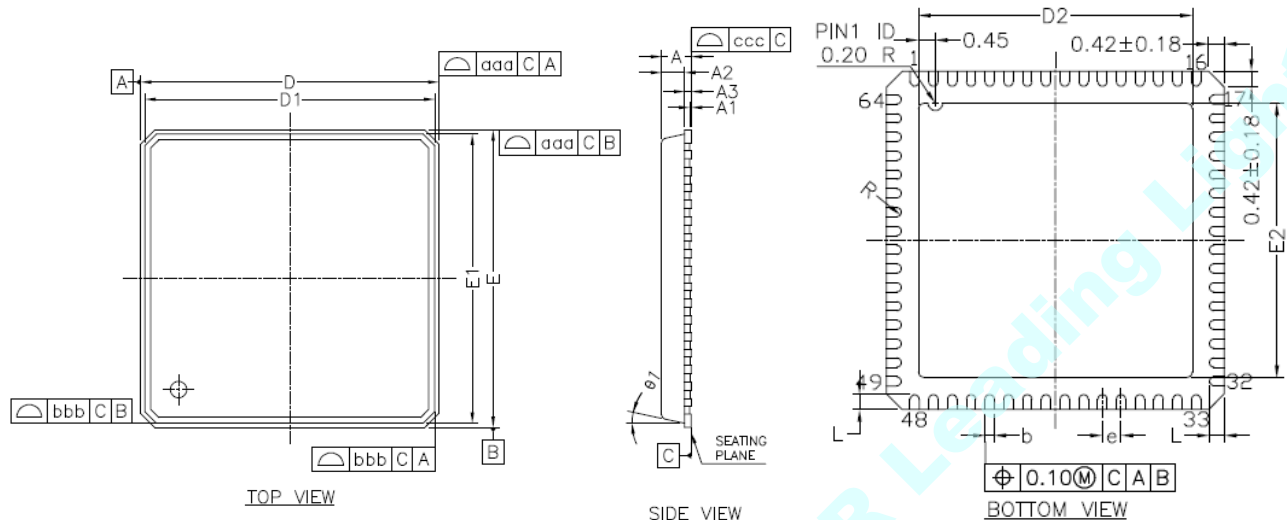


Figure 4: waveform of power on sequence

Symbols	Parameter	Min.	Typ.	Max.	Units
$t_{VCC2VCC}$	V_{CC} (90%) available after V_{CC} (90%) available	0	5	10	ms
$t_{VCC2VDD}$	V_{DD} (90%) available after V_{CC} (90%) available			90	ms
t_{RST}	RST (90%) ready after V_{CC} (90%) available	0			ms
$t_{25CLKOUT}$	25MHz clock available after RST#(90%) assert	0			ms
t_{PERST}	PCI Express Reset (90%) assert after RST#(90%) assert	100			ms
$t_{PECLKOUT}$	PCI Express Reference Clock output after RST#(90%) assert	101			ms

8. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	9.00 bsc			0.354 bsc		
D1	8.75 bsc			0.344 bsc		
D2	7.20	7.30	7.40	0.284	0.287	0.291
E	9.00 bsc			0.354 bsc		
E1	8.75 bsc			0.344 bsc		
E2	7.20	7.30	7.40	0.284	0.287	0.291
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 bsc			0.020 bsc		
θ1	0°	---	12°	0°	---	12°
R	0.09	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM (0.012 INCHES MAXIMUM)
3. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M, -1994.
4. DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. PACKAGE WARPAGE MAX 0.08 mm.
8. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
9. APPLIED ONLY TO TERMINALS.
10. PACKAGE CORNERS UNLESS OTHERWISE SPECIFIED ARE R0.175±0.025 mm.

Figure 5: Mechanical Specification

9. Top Marking Information

TBD

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